IN THE DRAWINGS:

Please enter two replacement sheets of drawings (Figures 3(a)-3(c) and Figure 4) that are attached to this Amendment.

REMARKS

The Office Action of October 22, 2007 has been received and its contents carefully considered.

In the response to the drawing objection, the present Amendment forwards a replacement sheet of drawings in which Figure 3(c) has been modified in several respects. One of these modifications is that a non-doped polysilicon arrangement 9 is now shown. The Amendment also forwards a new Figure 4, which illustrates an example in which the non-doped polysilicon arrangement covers an area larger than the total area of the N type and P type gates. In view of these revisions, it is respectfully submitted that the drawing objection should be withdrawn.

The present Amendment also revises the specification in view of the drawing changes.

Finally, the present Amendment revises independent claims 3 and 15, and adds two new dependent claims 20 and 21 to further protect the invention. It is noted that "smaller" in claim 15 has been corrected to "larger." The new dependent claims provide that the non-doped polysilicon arrangement is electrically disconnected from all of the transistors in the semiconductor device after it has been completed. Although this is not explicitly stated in the application, it is respectfully submitted that an ordinarily skilled person who had read the present application would have recognized that the inventor was in mental possession of what is recited in claims 20 and 21, so they do not constitute a new matter. That is, an ordinarily skilled person would have recognized that the reason why the non-doped polysilicon arrangement is produced is not so that it can be used as part of a circuit element.

The Office Action rejects claims 15-17 for obviousness based on US patent 5,783,850 to Liau et al (hereafter simply "Liau") in view of US patent 6,541,359 to Gabriel et al (hereafter simply "Gabriel") and US patent 4,989,057 to Lu. The Office Action takes the general position that Liau discloses an arrangement with an N type polysilicon gate electrode, a P type polysilicon gate electrode, and a non-doped polysilicon body 40. The Office Action also takes the general position that Gabriel discloses the use of end point detection during an etching process based on the etching of a non-doped polysilicon body. However, independent claim 15 provides that, not only is

end point detection of one of the stages of an etching process based on etching of a non-doped polysilicon arrangement, but also that this non-doped polysilicon arrangement occupies an area larger than the total area occupied by an N type polysilicon gate electrode and a P type polysilicon gate electrode.

The Office Action takes the general position that Lu teaches that the gate length/channel length of a transistor formed using an undoped portion of polysilicon as a gate is proportional to the breakdown voltage and holding voltage parameters of the device. Because of this, the Office Action takes the position that the gate length/channel length is considered to be a result effective variable where the result is the modification of the breakdown and holding voltage levels of the semiconductor device, so changing the size of the undoped portion of the polysilicon layer simply constitutes an optimization of the ranges. Applicant respectfully disagrees with this conclusion.

As a minor matter, it is respectfully submitted that Lu does not use undoped polysilicon as the gate electrode of his ESD protection transistor (see column 3, lines 57-59). More importantly, an ordinarily skilled person would want to use an ESD protection device with a breakdown voltage that is lower than the breakdown voltage of the transistors it protects. Consequently, an ordinarily skilled person would be likely to think that Lu's ESD protection transistor should have a relatively short channel length, or at least shorter than the channels of the devices it protects. It is therefore respectfully submitted that an ordinarily skilled person who wanted to optimize the parameters identified by Lu, in an ESD protection transistor, would not use a transistor with a non-doped polysilicon arrangement serving as a gate electrode where the non-doped polysilicon arrangement has a total area larger then the total area occupied by two other gate electrodes.

In addition, the passage in Lu identified by the Office Action, to support the conclusion that the size of an undoped portion of a polysilicon layer constitutes an optimization of ranges (that is, the passage at Lu's column 7, lines 40-55), refers to selecting a desired channel length of a protection device. However, the channel length of a transistor is not directly related to the area occupied by the transistor's gate electrode. For example, even if the length of the gate electrode is relatively small, the area occupied by the gate may be relatively large if the gate width is relatively large or if the number of gates is relatively large.

In short, it is respectfully submitted that the invention defined by independent claim 15 would not have been obvious from Liau, Gabriel, and Lu. The Office Action rejects independent claim 3 on the basis of these reference and also US patent 5,665,203 to Lee et al (hereafter simply "Lee"), but claim 3 also provides generally that a non-doped polysilicon arrangement is used for end point detection of a stage in an etching process and occupies an area larger than the total area occupied by two gate electrodes. Lu does not teach this, as discussed above, and neither does Lee.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention. They are therefore automatically patentable along with their independent claims. Nevertheless, new dependent claims 20 and 21 will now be briefly addressed.

Claims 20 and 21 provide that a non-doped polysilicon arrangement is electrically disconnected from all of the transistors in a semiconductor device. Even if the Lu reference were an adequate basis for optimizing parameters associated with the gate of an ESD protection transistor (despite the above argument to the contrary), this would not apply to a non-doped polysilicon arrangement that is not used as a part of a transistor in a circuit.

For the foregoing reasons, it is therefore respectfully submitted that this application is in condition for allowance. Reconsideration of the application is respectfully requested.

Respectfully submitted,

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